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ALPIDE, the Monolithic Active Pixel Sensor for the ALICE ITS upgrade

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ABSTRACT

A new 10 m^2 inner tracking system based on seven concentric layers of Monolithic Active Pixel Sensors will be installed in the ALICE experiment during the second long shutdown of LHC in 2019–2020. The monolithic pixel sensors will be fabricated in the 180 nm CMOS Imaging Sensor process of TowerJazz. The ALPIDE design takes full advantage of a particular process feature, the deep p-well, which allows for full CMOS circuitry within the pixel matrix, while at the same time retaining the full charge collection efficiency. Together with the small feature size and the availability of six metal layers, this allowed a continuously active low-power front-end to be placed into each pixel and an in-matrix sparsification circuit to be used that sends only the addresses of hit pixels to the periphery. This approach led to a power consumption of less than 40 mW cm^{-2}, a spatial resolution of around 5 μm, a peaking time of around 2 μs, while being radiation hard to some 10^{13} 1 MeV n_{eq}/cm^2, fulfilling or exceeding the ALICE requirements.

Over the last years of R & D, several prototype circuits have been used to verify radiation hardness, and to optimize pixel geometry and in-pixel front-end circuitry. The positive results led to a submission of full-scale (3 cm × 1.5 cm) sensor prototypes in 2014. They are being characterized in a comprehensive campaign that also involves several irradiation and beam tests. A summary of the results obtained and prospects towards the final sensor to instrument the ALICE Inner Tracking System are given.

1. Introduction

The planned upgrade of the ALICE inner tracking system (ITS) aims at improving the capabilities of ALICE in terms of read-out rate as well as in terms of position and momentum resolutions, especially of particles with low transverse momenta ($p_\perp < 1$ GeV/c). These targets result in requiring a very light detector with high granularity and read-out speed. Given that also the radiation load in ALICE is rather moderate, a design based on Monolithic Active Pixel Sensors (MAPS) was devised [1] and has been worked on over the last few years with the aim of installing the full system in 2019–2020.[1] This paper concentrates on the sensor chip itself and in particular on recent results from large-scale prototypes.

The new ALICE ITS layout comprises seven layers, three in the Inner Barrel (IB) and four in the Outer Barrel (OB) (schematically shown in Fig. 1) with some 10 m^2 of silicon.

With STAR's Heavy Flavor Tracker (HFT) and the ULTIMATE chip [2], MAPS entered high-energy physics applications [3,4]. The requirements of ALICE are more demanding in terms of radiation load, limit on power consumption and read-out times and ask for an improved sensor. Recent advancements in CMOS technology allowed these requirements (as shown below) to be met and since 2013, the ALICE ITS upgrade project is developing two sensor designs to address these requirements: MISTRAL-O, a rolling-shutter based chip and direct evolution of the ULTIMATE chip, and ALPIDE – a more aggressive approach aiming at reducing the power dissipation further by using a different read-out concept. Today, after thorough tests of its prototypes, ALPIDE serves as the project baseline.

Table 1 summarizes the sensor requirements. It has been shown that by fulfilling these requirements, a detector with an average material budget of 0.3% for its inner-most layers can be built [1]. However, any further optimization of power consumption would have a direct impact on the detector design as it would allow for a lighter detector by lowering the need of cooling and also power distribution.

2. ALPIDE

ALPIDE is a 1.5 cm × 3 cm large MAPS with 512 × 1024 (row × column) 28 μm × 28 μm pixels that are read out in a binary

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[1] LHC long shutdown two (LS2) according to revised LHC schedule.

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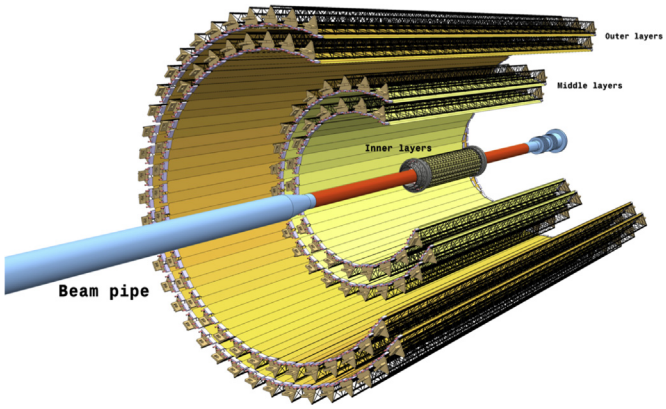

Fig. 1. Schematic layout of the upgraded ALICE ITS, extending from $r = 2.3$ cm to $R = 40$ cm, with η coverage of ± 1.22 (90% most-luminous region). (Picture taken from [1].)

Table 1
Sensor requirements for the ALICE ITS Upgrade for Inner Barrel (IB) and Outer Barrel (OB) [1].

Parameter	IB	OB
Sensor thickness (μm)	50	50
Spatial resolution (μm)	5	10
Dimensions (mm^2)	15 × 30	15 × 30
Power density ($mW\,cm^{-2}$)	300	100
Time resolution (μs)	30	30
Detection efficiency (%)	99	99
Fake hit rate[a]	10^{-5}	10^{-5}
TID radiation hardness[b] (krad)	2700	100
NIEL radiation hardness[b] ($1\,MeV n_{eq}/cm^2$)	1.7×10^{13}	10^{12}

[a] Per pixel and readout.
[b] Including a safety factor of 10, revised numbers w.r.t. TDR.

hit/no-hit fashion. It combines a continuously active, low-power, in-pixel discriminating front-end with a fully asynchronous, hit-driven combinatorial circuit.

2.1. Technology

The technology chosen for the ALICE ITS upgrade (both ALPIDE and MISTRAL-O) is TowerJazz's 180 nm CMOS Imaging Process.[2] The design of ALPIDE takes full advantage of the process features offered, in particular of the high integration density given by the availability of six metal layers and the small structure size as well as of the deep p-well. The latter allows PMOS transistors to be fabricated on a p-type epitaxial layer without penalizing the charge collection, by shielding their n-well from the epitaxial layer as shown schematically in Fig. 2 [5]. The availability of sizable CMOS circuitry inside the pixel matrix allowed the read-out concept to be changed moving away from the classical rolling shutter readout that is usually employed in MAPS towards more power-efficient schemes.

Another important feature is the availability of high-resistive ($> 1\,k\Omega\,cm$) epitaxial layers that allow for better charge collection. It is also possible to moderately ($< 10\,V$) reverse bias the substrate, which has been proven to significantly improve the charge collection [6,8].

2.2. In-pixel circuitry

Figs. 3 and 4 depict schematically discriminator circuit and the functioning of the ALPIDE in-pixel front-end circuitry, respectively.

[2] www.jazzsemi.com

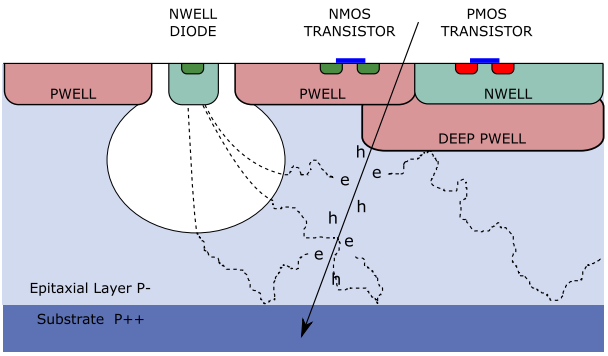

Fig. 2. Schematic view of the well-structure used for ALPIDE and the corresponding charge collection. (Picture taken from [1].)

The in-pixel circuitry consists of a continuously active discriminating amplifier and a multiple-event memory into which data may be strobed. The rise time of the amplifier is below 2 μs and defines the event time resolution while its shaping time is longer and makes it act as an analogue delay line. This allows data to be discriminated and strobbed with a trigger latency of some 2 μs into the in-pixel buffers in a global shutter mode of operation. Strobing can also be done with fixed spacing and over longer periods, making the circuit record data continuously.

2.3. Matrix read-out and system level integration

The in-pixel multiple-event memory is read out asynchronously by means of a priority encoder circuit in each double column. This is both fast and power efficient as the expected occupancies are low and only hit pixels are read out in a hit-driven fashion [9]. Data is collected at the periphery and shipped off detector by means of a high-speed serial link.[3] The sensor is flip-chip mounted to the supporting printed circuit board using laser-soldered solder balls that are distributed over the full area of the chip.

3. Prototypes

Since 2012, several prototype circuits have been developed and characterized to address different parts and aspects of the final ALPIDE chip. The first generation of prototypes (called “Explorer”) was addressing the charge collection properties of the underlying CMOS process and was used to optimize the sensing node geometry [7]. The next generation in 2013 (“pALPIDEss”) was prototyping the new low-power in-pixel amplification and discrimination front-end, which marks the distinctive feature of the ALPIDE [10].

3.1. pALPIDE-1

Since 2014, a full-scale sensor prototype (“pALPIDE-1”, Fig. 5) is available and used to qualify the development in large-scale devices. The results obtained with pALPIDE-1 form the remainder of this paper.

Table 2 compares the pALPIDE-1 prototype with respect to the final ALPIDE chip. Subsequent prototypes pALPIDE-2, and pALPIDE-3 will continue in adding the remaining features, notably the high-speed serial interface and the in-pixel multiple-event memory. pALPIDE-1 features three different sensing node

[3] The chip also supports a mode where data of six adjacent chips is collected by one sensor acting as master; more in detail in [11] (this issue).

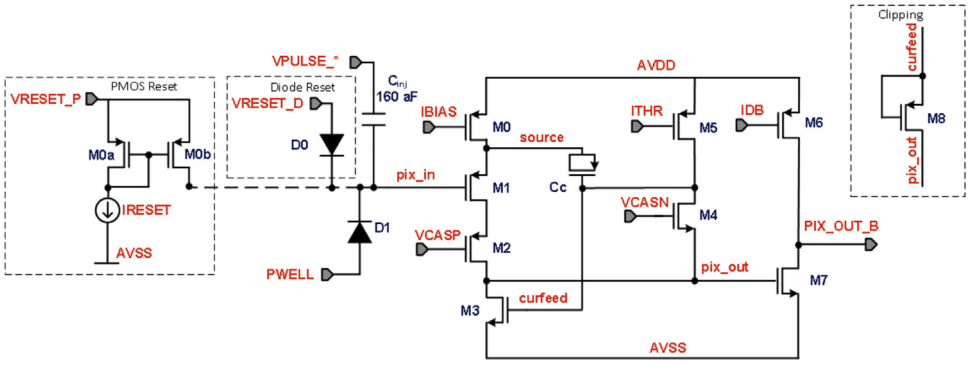

Fig. 3. Reset, amplification and discrimination circuit of (p)ALPIDE.

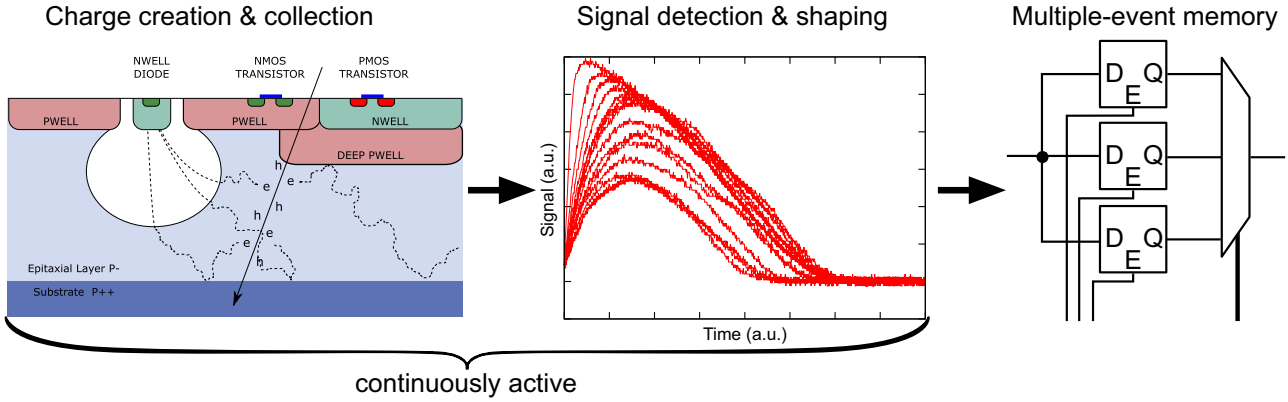

Fig. 4. Principle of operation of ALPIDE in-pixel circuitry.

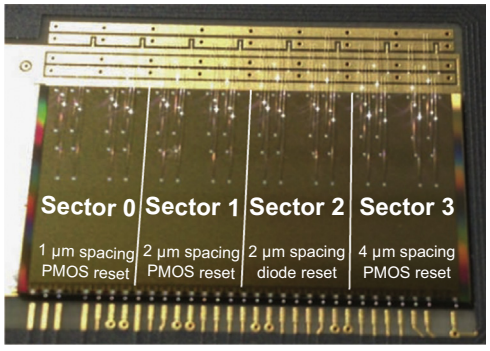

Fig. 5. Photograph of the pALPIDE-1 indicating its splits. Here the circuit is wire-bonded to a carrier PCB using the large solder pads distributed over the active area, which is foreseen to be soldered directly to the flex printed circuit in the final detector.

Table 2
Differences between pALPIDE-1 and ALPIDE.

Parameter	pALPIDE-1	ALPIDE
In-pixel multiple-event buffers	1	3
Read-out port	8-bit parallel	Serial
Read-out link bandwidth (Gbit/s)	0.32	1.2
Pixel geometries	3	1
Pixel resetting mechanism	Diode, PMOS	tbd
Matrix read-out circuit	Full custom	Standard cell
Master-slave interface	Missing	Implemented
Power density (mW/cm^2)	40	<40

geometries, which differ by how much space is kept free between the collection electrode and the surrounding p-well. Previous results from analogue prototypes gave strong indication that more spacing helps to reduce input capacitance and the charge spread, both effects attributed to a larger depleted volume. They, however, can also lead to a worsening of the spatial resolution. Spacings of 1, 2, and 4 µm have been tried. In addition, two resetting mechanisms are investigated: one utilizing a forward diode and one using a PMOS transistor (see Fig. 3).

4. Test beam results

After successful laboratory tests at several institutes participating in the ALICE ITS upgrade project, pALPIDE-1 has been brought to a number of test beam facilities, namely DESY (5 GeV e^- in Hamburg, Germany), BTF (450 MeV e^- in Frascati, Italy), PAL (60 MeV e^- in Pohang, Korea), PS (6 GeV π^- at CERN) and SPS (120 GeV π^- at CERN). There, detection efficiencies and spatial resolutions were measured with a telescope made of 6–7 planes of pALPIDE-1 sensors arranged as shown in Fig. 6. Here results from the CERN PS will be shown.

4.1. Detection efficiency and fake hit rate

Treating the middle planes as devices under test (DUTs), and tracking particles using the outer planes, the detection efficiencies for different bias settings of the sensor were obtained. Fig. 7 shows the detection efficiency as a function of the threshold current I_{thr}. The figure combines these measurements with the fake hit rate measured per event and pixel in the laboratory. Here the 20 most noisy pixels (which corresponds to ≈ 0.15 and hence has only a negligible influence on the detection efficiency) are masked. It should be noted that the chip has dedicated masking registers within each pixel for this purpose.

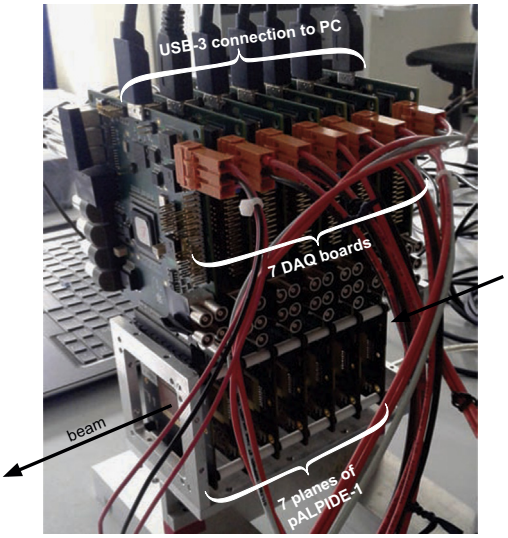

Fig. 6. The pALPIDE-1 test beam telescope set-up.

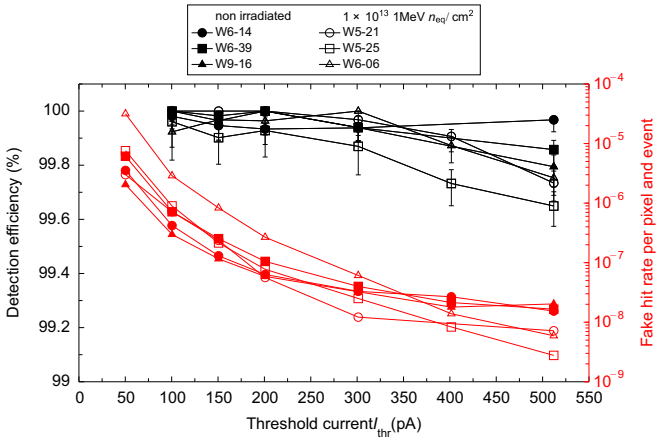

Fig. 7. Detection efficiencies and fake hit rates of pALPIDE-1 shown for different dies as well as before and after neutron irradiation. Data is for sector 2 with a reverse bias voltage of −3 V.

The obtained results show a large operational margin with detection efficiencies well above 99% at fake hit rates significantly below 10^{-5} for several sensors.

4.2. Cluster size and spatial resolution

Average cluster sizes and spatial resolutions are shown in Fig. 8. Here, a sector with 2 µm spacing showed the best performance, since the clusters are large enough to provide sub-pixel resolution (i.e. better than pitch/$\sqrt{12}$). This can nicely be seen looking at the cluster size as a function of impinging point as depicted in Fig. 9 for an area of 2 × 2 pixels (the elementary layout cell).

4.3. Radiation tolerance

Figs. 7 and 8 also show results before and after neutron irradiation to a level of up to 10^{13} 1 MeV n_{eq}/cm^2 to assess a possible degradation of detection performance. One hardly sees any irradiation-related degradation of the performance at these irradiation levels. Still, the slightly lower detection efficiencies after irradiation as well as the smaller average cluster sizes that are observed systematically in several measurements can be attributed to first signs of radiation damage. Measurements with higher irradiation doses are underway to determine the limits.

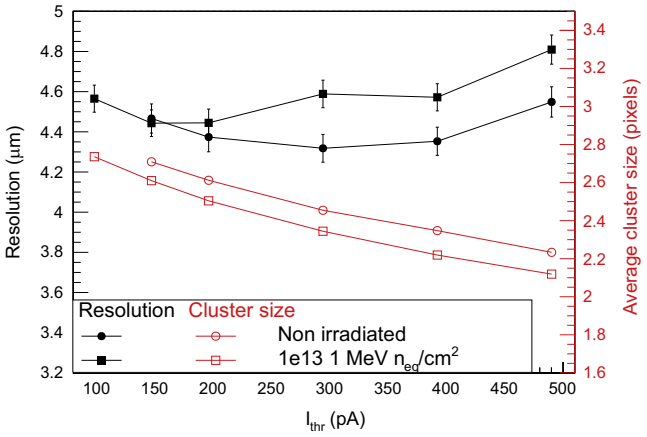

Fig. 8. Cluster sizes and spatial resolution of pALPIDE-1 shown for different dies as well as before and after neutron irradiation. Data is for sector 2 with a reverse bias voltage of −3 V.

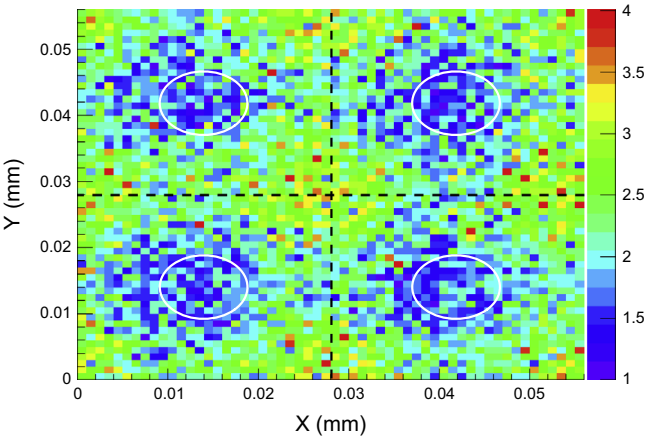

Fig. 9. Cluster sizes dependent on impact point within 2 × 2 pixels. When particles hit the sensor at the center, the average size is below 2, rising to 3.5 in cases where the particle impinges the sensor at the corner of a pixel. Data is for sector 2 with a reverse bias voltage of −3 V.

5. Conclusion

With the pALPIDE-1, the ALPIDE chip development underwent a crucial step towards its finalization. The performance of the prototypes has been assessed with a multitude of test beams, supplemented with laboratory tests before and after neutron irradiation. The sensor shows a detection efficiency above 99%, a fake hit rate much better than 10^{-5} and a spatial resolution of around 5 µm over a large range of operational settings. The operational margin is kept even after neutron irradiation to 10^{13} 1 MeV n_{eq}/cm^2.

Acknowledgments

We would like to thank the host institutes, notably DESY, BTF Frascati, Pohang, CERN, for their excellent support when carrying out test beams.

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